Ambrish K Varma
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Objective: Pursue a PhD. in the Computer Engineering field in the specific areas of signal integrity and noise that is encountered during chip design and simulation.

Summary: Over 3 years of work experience in the hardware industry that includes more than 2 years of industry level experience in digital design that involves circuit design and programming in Verilog/VHDL for simulation and synthesis with verification.

Experience:

May 2002 – present : Enrolled in the PhD program working on Input/Output Buffer Information Specification (IBIS). Coded S2IBIS3 (Spice to Ibis version 3), a program to convert spice netlist to IBIS models. Also involved in doing SSN analysis on IBIS models and developing better noise representation in IBIS models.

Mar 2001 – Feb 2002: Design Engineer in the Wireline Access (Litespan) division of **Alcatel USA** based in Raleigh, NC. Responsibilities include FPGA Design, Verification and Lab testing. Worked on the Backplane ADSL Multi-port Bus Interface (**BAMBI**) FPGA, designing and implementing specific aspects of the FPGA such as

- Digital PLL,
- Multi-port and single-port loop back,
- Designing test modules to test various interfaces (memory interface, UTOPIA interface and High Speed Cell Bus interface) and
- Writing Perl scripts to automate the timing analysis of the FPGA.

The FPGA supports **ATM** Traffic on 4 ports and is designed using a Xilinx Virtex E FPGA. **Verilog** and **VHDL** were simultaneously used. **Xilinx Alliance 3.3i** and **Synplify 6.0.0** were used to synthesize the design.

Aug 2000 – Mar 2001: Research Assistant, ECE dept. NC State University. Advisor: Dr. Paul Franzon. Worked on bringing package and other layout design issues into IC tools for Multi-Chip modules. The Seamless High Off Chip Connectivity (**SHOCC**) technology allows bump arrays and interconnects to be reassigned from chip to package. Research involved Designing Tech Library for **Cadence Virtuoso** Layout package, **DRC**, **Extraction** and **LVS** decks for verification, programming in **SKILL**. The final deliverables included the Technology Library, DRC, Extraction and LVS diva Decks and a working example that was simulated using **HSPICE**. The work was funded by **Intarsia Corp,** a Fremont CA based company.

Jun 2000 – Aug 2000: Summer Co-op at IBM Corp. Worked in the Microelectronics Division in the verification team for their network processor. Responsibilities include

- Simplifying the process of test case generation through scripting in Perl to generate test cases.
- Helped in testing the N/W processor and to correctly document the different registers.

Jan 2000 – May 2000: Completed 128 bit encryption project at NC State University. Implemented the RC6 block cipher using Verilog. The design had 2 modules, the key generation module and the Enc/Dec module. **Synopsys** was used to synthesize the Enc / Dec engine.

Aug 1999 - Dec 1999: Assistantship in the Center for Advanced Computer Studies (CACS) at University of Louisiana at Lafayette, (ULL) LA. Designed a MAC (Multiplier Accumulator) chip using **MAGIC.** The circuit was tested using **HSPICE**. The main objective was to obtain a high speed and a low power MAC unit. Project was rated as the best-completed VLSI project by the course coordinator.

Jun 1998 – Aug 1999: Part time employment at BRI Australia Ltd. as a Technical Assistant and after graduation, Research Engineer. Worked on Online Monitoring and Control of Manufacturing process. Work involved integration of control hardware and software.

Computer Skill: ***Languages*** **–Verilog HDL, VHDL, Skill, Perl, C, C++, JAVA**

Operating Systems – UNIX, AIX, Windows, DOS – 5

Software Packages – Cadence, Magic, Synopsys, HSpice, Synplify 6.0.0, Xilinx Alliance 3.3i, Altera Quartus II, RCS, Mathcad Labview.

Projects:

- **Integrated Control and Optimization System– Hardware and Software. April 1998 – November 1998, UWSN, Australia**

  Final Year Project for Successful completion of BEng. Monitor and Control an on-line manufacturing process in a commercial bakery using a PLC along with a proximity and a color sensor. Software was written to communicate with the PLC, the sensors and the Computer. The software was written using **Visual Basic** (Ver 5). This Project was completed at BRI Australia Ltd. and was ranked among the first 2 projects of the university.

- **Undergraduate Vacation Scholarship, Quality Wheat CRC Dec 1997 - April 1998**

  Completed a preliminary test of feasibility of the Online Continuous Color Meter for Monitoring the Color of Product Leaving the Oven. Project Completed at BRI Australia Ltd.
- **Nepean Summer Research Award, University Of Western Sydney, Dec1996 – March 1997**

  Built a Carbon Monoxide and Combustible Gas Sensing System. Project Completed at BRI Australia Ltd**.**
- **Design and Construction of a Digital Alarm Clock, UWSN, 1997**. Used programmable GALs to design a fully functional digital alarm clock as part of course work for Digital System project in year 3 of degree.

Education:

- MS in Computer Engineering. Feb 2001.

  North Carolina State University at Raleigh, North Carolina. GPA 3.667/4.0

  Courses

  VLSI Design, ASIC (Application Specific IC Design), Computer Networks, Computer Architecture, ATM, Broadband Internet Access (DSL, Cable modems, Optical N/W), Wireless, Network Security.

- BE Electrical Engineering, (Honors), April 08 1999

  University of Western Sydney, Nepean (UWSN), Sydney, NSW, Australia. GPA 3.6/4.0

  Courses

  Digital Systems, Circuit Theory, Electromagnetics, Engineering Software Principles, Electronics, Antennas and Propagation, Control Systems, Power Systems, Filter, Communications, Sensors Measurements and Data Acquisitions, Optical Fiber Engineering, Electromagnetic Compatibility, Advanced Electronics.

Honors and Activities:

Active member IEEE since 1998.

Founder - President of the COMSTAT Association (Computer and Statistic Department association) University of Allahabad 1994.

Editor-in-Chief of IMPRESSIONS - Annual Magazine of COMSTAT, 1994.

Vice President, Literary Association of St. Joseph College, Allahabad, India, 1992.

Editor-in-Chief of HORIZON - Annual Magazine of Literary Association St. Joseph's College, India, 1992.

References: Furnished upon request.

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